IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Tuning circuit for tuning a filter stage, which has an RC element ~~(1)~~ with an RC time constant ~~(τ)~~, with the RC time constant ~~(τ)~~ being the product of the resistance of a resistor ~~(R1)~~ in the RC element ~~(1)~~ and the capacitance of a capacitor ~~(C1)~~, which is connected in series with the resistor ~~(R1)~~, in the RC element ~~(1)~~, having:

   (a) a comparator ~~(10)~~ for comparison of the voltage which is produced at the potential node ~~(4)~~ between the resistor ~~(R1)~~ and the capacitor ~~(C1)~~, with a reference ground voltage; and having

   (b) a controller ~~(15)~~ which varies the charge on the capacitor ~~(C1)~~ in the RC element ~~(1)~~ until the comparator ~~(10)~~ indicates that the voltage which is produced at the potential node ~~(4)~~ is equal to the reference ground voltage, with the controller ~~(15)~~ switching a capacitor array ~~(26)~~ as a function of the charge variation time, which capacitor array ~~(26)~~ is connected in parallel with the capacitor ~~(C1)~~ in the RC element ~~(1)~~, in order to compensate for any discrepancy between the RC time constant ~~(τ)~~ of the RC element ~~(1)~~ and a nominal value.

2. (Currently Amended) Tuning circuit according to Claim 1, ~~characterized in that~~ wherein the filter stage is contained in an integrated analog filter ~~(3)~~.

3. (Currently Amended) Tuning circuit according to Claim 1, ~~characterized in that~~ wherein the controller ~~(15)~~ has a sequence controller ~~(14)~~ for driving switches which are provided in order to vary the charge on the capacitor ~~(C1)~~ in the RC element ~~(1)~~.

4. (Currently Amended) Tuning circuit according to Claim 3, ~~characterized in that~~ wherein the switches are integrated in the analog filter ~~(3)~~.

5. (Currently Amended) Tuning circuit according to Claim 4, ~~characterized in that~~ wherein the switches are CMOS switches.

6. (Currently Amended) Tuning circuit according to Claim 3, ~~characterized in that~~ wherein the sequence controller ~~(14)~~ has a digital counter for measurement of the charge variation time.

7. (Currently Amended) Tuning circuit according to Claim 6, ~~characterized in that~~ wherein the digital counter for the sequence controller ~~(14)~~ is clocked by means of an external clock signal ~~(CLK)~~.

8. (Currently Amended) Tuning circuit according to Claim 7, ~~characterized in that~~ wherein the digital counter for the sequence controller ~~(14)~~ counts the number ~~(Z)~~ of clock cycles from the external clock signal between reception of a start signal and reception of a stop signal which is received from the comparator ~~(10)~~.

9. (Currently Amended) Tuning circuit according to Claim 1, ~~characterized in that~~ wherein the controller ~~(15)~~ has a memory ~~(16)~~ which is connected to the sequence controller ~~(14)~~.

10. (Currently Amended) Tuning circuit according to Claim 9, ~~characterized in that~~ wherein a coded tuning control signal for switching the capacitor array ~~(26)~~ is stored in the memory ~~(16)~~ for each count ~~(Z)~~ of the digital counter.

11. (Currently Amended) Tuning circuit according to Claim 10, ~~characterized in that~~ wherein the capacitor array ~~(26)~~ has two or more tuning capacitors ~~(28-i)~~ which are connected in parallel with the

capacitor ~~(C1)~~ in the RC element ~~(1)~~ as a function of the coded tuning control signal.

12. (Currently Amended) Tuning circuit according to Claim 11, ~~characterized in that~~ wherein the capacitances of the tuning capacitors ~~(28-i)~~ are weighted multiples of a basic capacitance ~~(C_{basic})~~.

13. (Currently Amended) Tuning circuit according to Claim 1, ~~characterized in that~~ wherein the capacitor array ~~(26)~~ is integrated in the filter stage.

14. (Currently Amended) Tuning circuit according to Claim 3, ~~characterized in that~~ wherein the integrated analog filter can be switched between a normal filter mode and a tuning mode by means of switches which are controlled by the sequence controller ~~(14)~~.

15. (Currently Amended) Tuning circuit according to Claim 1, ~~characterized in that~~ wherein the filter stage has a completely differential operational amplifier ~~(29)~~.

16. (Currently Amended) Tuning circuit according to Claim 15, ~~characterized in that~~ wherein the completely differential operational amplifier ~~(29)~~ has a first signal input which is connected to a potential node ~~(4)~~ in a first RC element ~~(1)~~, a second signal input which is connected to the potential node ~~(5)~~ in a second RC element ~~(2)~~, a first signal output which is fed back via the capacitor ~~(C1)~~ in the first RC element ~~(1)~~ to the first signal input, and a second signal output which is fed back via the capacitor ~~(C2)~~ in the second RC element ~~(2)~~ to the second signal input.

17. (Currently Amended) Tuning circuit according to Claim 16, ~~characterized in that~~ wherein the capacitor ~~(C1)~~ in the first RC element ~~(1)~~ is charged by means of switches which are controlled by

the sequence controller ~~(14)~~, and the capacitor ~~(C2)~~ in the second RC element ~~(2)~~ is discharged by means of switches which are controlled by the sequence controller ~~(14)~~, until the voltages which are produced at the potential nodes ~~(4, 5)~~ in the two RC elements ~~(1, 2)~~ are of equal magnitude.

18. (Currently Amended) Tuning circuit according to Claim 17, ~~characterized in that~~ wherein the comparator ~~(10)~~ has:
- a first signal input ~~(8)~~ which is connected to the potential node ~~(4)~~ in the first RC element ~~(1)~~,
- a second signal input ~~(9)~~ which is connected to the potential node ~~(5)~~ in the second RC element ~~(2)~~, and
- an output ~~(11)~~ for emitting a stop signal to the sequence controller when the voltage which is applied to the first signal input ~~(8)~~ is equal to the voltage which is applied to the second signal input ~~(9)~~.

19. (Currently Amended) Tuning circuit according to Claim 18, ~~characterized in that~~ wherein the counter which is contained in the sequence controller ~~(14)~~ records the time until the voltages which are applied to the two signal inputs ~~(8, 9)~~ of the comparator ~~(10)~~ are of equal magnitude.

20. (Currently Amended) Tuning circuit according to Claim 1, ~~characterized in that~~ wherein the filter stage has an operational amplifier ~~(33)~~ whose first signal input is connected to the potential node ~~(4)~~ in the RC element ~~(1)~~ and whose signal output ~~(36)~~ is fed back via the capacitor ~~(C1)~~ in the RC element ~~(1)~~ to the first signal input ~~(8)~~.

21. (Currently Amended) Tuning circuit according to Claim 20, ~~characterized in that~~ wherein the comparator ~~(10)~~ has:
- a first signal input ~~(8)~~, which is connected to the signal output ~~(36)~~ of the operational amplifier ~~(33)~~,

- a second input ~~(9)~~, to which the reference ground voltage is applied, and
- an output ~~(11)~~ for emitting a stop signal, to the sequence controller, when the voltage which is applied to the first input is equal to the reference ground voltage.

22. (Currently Amended) Tuning circuit according to Claim 21, ~~characterized in that~~ wherein the second input ~~(9)~~ of the comparator ~~(10)~~ can alternatively be connected by means of switches ~~(44, 45)~~ which are controlled by the sequence controller ~~(14)~~ to a first reference voltage source ~~(31)~~ which generates a first reference voltage, or to a second reference voltage source ~~(32)~~ which generates a second reference voltage.

23. (Currently Amended) Tuning circuit according to Claim 22, ~~characterized in that~~ wherein the capacitor ~~(C1)~~ in the RC element ~~(1)~~ can alternatively be connected by means of switches ~~(44, 45)~~ which are controlled by the sequence controller ~~(14)~~ to the first reference voltage source ~~(42)~~ in order to charge the capacitor in a first direction, or to the second reference voltage source in order to charge the capacitor ~~(C1)~~ in the opposite direction to the first direction.

24. (Currently Amended) Tuning circuit according to Claim 22 ~~or 23, characterized in that~~ wherein the capacitor ~~(C1)~~ has its charge varied by means of the switches which are controlled by the sequence controller ~~(14)~~, until the first reference voltage is applied to the first input ~~(8)~~ of the comparator ~~(10)~~, and the capacitor ~~(C1)~~ then has its charge varied in the opposite direction by means of the switches which are controlled by the sequence controller ~~(14)~~ until the second reference voltage is once again applied to the first input ~~(8)~~ of the comparator ~~(10)~~.

25. (Currently Amended) Tuning circuit according to Claim 24, ~~characterized in that~~ wherein the counter which is contained in the

sequence controller ~~(14)~~ records the overall time for the charge variation and for the opposite charge variation of the capacitor ~~(C1)~~.

26. (Currently Amended) Tuning circuit according to Claim 2, ~~characterized in that~~ wherein the analog filter is an anti-aliasing filter.

27. (Currently Amended) Tuning circuit according to Claim 26, ~~characterized in that~~ wherein the analog filter is an xDSL anti-aliasing filter.

28. (Currently Amended) Tuning circuit according to Claim 2, ~~characterized in that~~ wherein the analog filter is a biquad filter.

29. (Currently Amended) Tuning circuit according to Claim 2, ~~characterized in that~~ wherein the analog filter is completely differential.

30. (Currently Amended) Tuning circuit according to Claim 3, ~~characterized in that~~ wherein the analog filter has two or more filter stages.

31. (Currently Amended) Method for tuning a filter stage which contains an RC element with an RC time constant, with the RC time constant ~~(τ)~~ being the product of the resistance of a resistor ~~(R1)~~ in the RC element ~~(1)~~ and the capacitance of a capacitor ~~(C1)~~, which is connected in series with the resistor ~~(R1)~~, in the RC element ~~(1)~~, with the method having the following steps:

(a) variation of the charge on the capacitor ~~(C1)~~ by at least one RC element ~~(1)~~ in the filter stage;

(b) measurement of the charge variation time until the voltage which is produced at the potential node ~~(4)~~ between the resistor ~~(R1)~~ and the capacitor ~~(C1)~~ in the RC element ~~(1)~~ reaches a reference ground voltage;

(c) switching a capacitor array ~~(26)~~, which is connected in parallel with the capacitor ~~(C1)~~ in the RC element ~~(1)~~, as a function of the measured charge variation time, in order to compensate for any discrepancy between the RC time constant ~~(τ)~~ of the RC element ~~(1)~~ and a predetermined nominal value ~~(τ_{NOM})~~.

32. (Currently Amended) Method according to Claim 31, ~~characterized in that~~ wherein the capacitor ~~(C1)~~ in the RC element ~~(1)~~ is charged to a specific first reference ground voltage before the tuning of the filter stage.

33. (Currently Amended) Method according to Claim 32, ~~characterized in that~~ wherein, in order to tune the filter stage, the charge on the capacitor ~~(C1)~~ is varied until the voltage which is dropped across the capacitor ~~(C1)~~ is equal to a second reference ground voltage, and it is then charged in the opposite direction until the voltage which is dropped across the capacitor ~~(C1)~~ is once again equal to the first reference ground voltage.

34. (Currently Amended) Method according to Claim 33, ~~characterized in that~~ wherein the two charge variation times for varying the charge on the capacitor ~~(C1)~~ are measured as an overall time.

35. (Currently Amended) Method according to Claim 33, ~~characterized in that~~ wherein a capacitor ~~(C1)~~ in a first RC element ~~(1)~~ is charged to a first reference ground voltage before the tuning of the filter stage, and a capacitor ~~(C2)~~ in a second RC element ~~(2)~~ is charged to a second reference ground voltage before the tuning of the filter stage, with the capacitor ~~(C1)~~ in the first RC element ~~(1)~~ being discharged, and the capacitor ~~(C2)~~ in the second RC element ~~(2)~~ being charged, until the voltage across the two capacitors ~~(C1, C2)~~ is of equal magnitude.

36. (Currently Amended) Method according to Claim ~~37~~ 35, ~~characterized in that~~ wherein the charge variation time until the two voltages across the two capacitors ~~(C1, C2)~~ are of equal magnitude is measured.